Scaling Trend of CMOS based RF Circuits

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Abstract: With the cutting edge of technology, the number of portable devices using wireless equipment is increasing significantly and therefore, design and implementation of high-performance 4G digital the system is in high demand and challenging task. Radio frequency (RF) circuits are the interface devices between wireless equipment and antenna. In the past, RF circuits were made with large analog components such as transistors, coils, etc. By development of Complementary metal oxide semiconductor (CMOS) technology, CMOS transistors came to function. However, the scaling of devices were accelerated due to using simple CMOS technologies. The scaling trend was continued therefore, current leakage, power consumption usage became undeniable issues, and hence, this review paper is considering the research-taking place in CMOS scaling based RF modules in recent years [1-22]. The review paper shows changing parameters in CMOS technology is not an efficient solution for transistor fabrication and innovations on materials and structure are required to address the fabrication problems.

1. INTRODUCTION

By developing wireless technologies during recent years, the great impact of wireless equipment can be felt due to the amazing growth of mobile devices. In other words, wireless circuits have become the fundamental of many telecommunication instruments

3]. Clearly, the wireless equipment is consisting of the radio RF circuit, which is the interface between antenna and wireless equipment. In conventional RF products, bipolar and gallium arsenide (GaAs) components have been used in the variant frequency ranges, however, recently the CMOS technology is able to make RF circuits for any of this frequency ranges. With the advance, CMOS based RF technology, high efficient digital system formulated and designed in terms of chip size and low power consumption. Yet the trend showed a narrow improvement until 2003 that the chief technology officer of IBM Microelectronics announced the scaling is dead. [4]. Certainly, in CMOS based RF circuit design, reducing the size of transistor beyond 22nm not only had not sufficient efficiency but also had harmful effects on the circuit performance such as power dissipation and lessen the throughput [5]. Therefore, Advanced CMOS technologies are in high demand to overcome the challenging task. There are some concepts such as silicon on insulator (SOI), strained silicon, high-k (advanced dielectric materials), and multi-gate transistors that can help the scientist to face with the problems associated with scaling [6, 7]. PARAMETERS FOR CMOS BASED RF CIRCUITS

1.1. CMOS RF Performance

Transit frequency (f_t) is one of the foremost known parameters of transistors. It is defined by drain current divided by gate current when v_{ds} is zero. In other words, f_t is the frequency where the small-signal-current-gain of the device drops to unity while the source and drain terminals are grounded.

The impact of parasitic output (parallel) and input (series) of the transistor is ignored due to the definition (v_{ds}= 0). This definition is suitable for transistors where has a low drain-source small-signal output (conductanceg_{ds}) towards the load (admittance g_l). However, the literature showed that transistors is much small-signal voltage gain is not achievable. The coefficient g_m/g_{ds} (high intrinsic voltage gain) can control and limit the maximum voltage gain in the circuits [8]. As far as researches concerned, this coefficient is not compatible with lots of high-speed structures witch functionally riles on voltage gain. Hence, using just f_t for designing the RF circuits is meaningless due to having large g_{ds}Therefore in addition to f_t another parameter is required to characterize the design.

One parameter is g_m/g_{ds} coefficient and another one is the maximum frequency of oscillation (f_{max}) which is the frequency where power gain drops to 0 dB [9]. f_{maxt} is varied from f_t.

1.2. CMOS Scaling

The trend of scaling CMOS circuits from 350*nm* to 10*nm* is shown in Fig.1 (1997 - 2020).

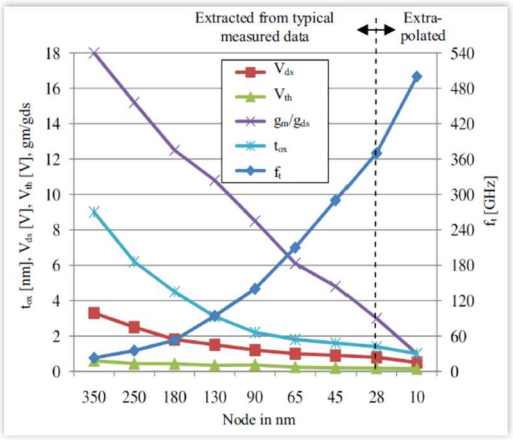

Fig. 1. CMOS scaling vs transistor parameters [4]

From 350 *nm* until around 45*nm*, Equ. (1) is utilizing for scaling:

$$f_t \sim \frac{1}{L_g^2} \quad (1)$$

where L_g corresponds to the length of the gate. Equ. (1) provides the concept of reverse relation between the length of the gate and transit frequency due to saturation effect and short length channel.

Equ. (1) is changed to $f_t \sim \frac{1}{L_g}$ around 45*nm* and for more scaling (around 10*nm*) the equation will be $f_t \sim \frac{1}{L_g^n}$ where 0 < n < 1.Hence, decreasing the gate length is not an efficient way of designing the transistors by scaling below 45*nm* due to high electrical field in a short channel.

To avoid the effect of the electrical field in the channel the efficient way is to decrease V_{Ds} alternatively by reducingL_g; until V_{Ds} reach approximately 0.5V.

Lessen V_{Ds} has some disadvantages such as reducing the out coming power of RF. In addition, since 250*nm* to 45*nm,* due to the coefficient $g_m/g_{ds}$is decreasing by 34% and the worst case is that by reducing the scale to 10*nm* the coefficient g_m/g_{ds} descend to unity approximately that is harm for RF system module. Furthermore, there is fabrication problem of 10*nm* scaling such as gate oxide layer thickness; It must be below 1*nm* to control the channel sufficiently, which cause the current leakage between gate and source or drain and lead to more power dissipation[10]. Hence, this paper results by changing this parameter, it is impossible to design an efficient RF amplifier and innovations on materials and structure are required to address the problems.

2. ADVANCED TECHNIQUES FOR CMOS SCALING USING IN RF MODULES

As it discussed, scaling CMOS is a challenging task and there are several techniques to mitigate the issues as such: *A) Strain Silicon (SSi)*

Strained silicon is a practical way to improve electron and hole motilities of the channel region. This method improves the transistor current (Ion), and therefore, helps factories to scale the transistors by keeping the gain performance. Power consumption reduction of CMOS transistors using SSI technique leads to reduce power dissipation [11, 12].

When silicon atoms are stretched more than common interatomic length, the generated structure is called strained silicon. This structure is created by deposition a small layer of silicon-germanium (SiGe) on the surface of the silicon to make the virtual layer, then a thick layer of Si is grown on the virtual surface to make the strained structure, which has higher carrier mobility. Fig.2 shows the strained silicon structure.

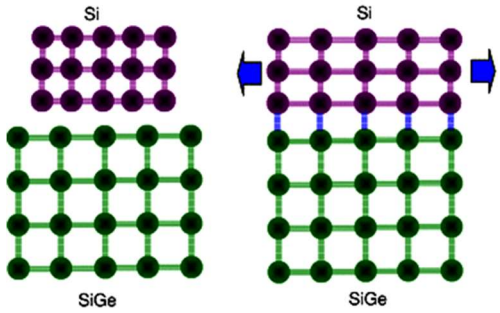

Fig. 2. Illustration of strained silicon structure

Lower fan-out, lower power consumption, and higher speed are some advantages of this structure due to having more carrier mobility [13].

2.1. B) Silicon on isolation *(SOI) Technology*

SOI is an efficient method for CMOS scaling. In this method, a thin layer of an insulator such as separates active layer and substrate from each other SiO_2. Therefore, this combination makes the transistor

relax of enhancing L_g during scaling [14]. SOI offers high performance due to the separation of active layer and substrate, high resistivity can be selected without any effect on V_{th} , low power consumption due to reducing the leakage current and higher speed compared to traditional silicon components [15]. Fig.3 presents the SOI structure.

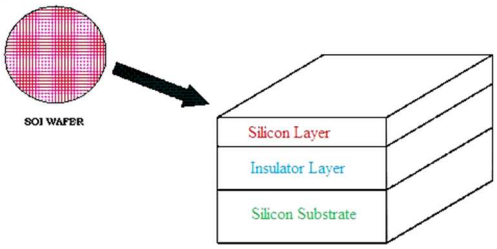

Fig. 3. SOI Structure

However, tunneling in a small layer of oxide can cause the current leakage when scaling down (T_{ox}) the transistor. Leakage can cause higher noise generation in the circuit and reduce the performance of the RF circuit. This problem is addressing by using high dielectric materials (high barrier gate oxide) such as zirconium (ZrO_2) or hafnium oxide (HfO_2). Unfortunately, impurities and traps affect these materials, which influence the RF performance. Therefore, these materials are not suitable for use in RF circuits [16, 17].

2.2. C) Complementary Of SOI and Strained Silicon

The complementary structure has both advantages of SOI and strained silicon due to the effect of an insulator under the active region. Insulator separate active layer and buried insulator under active channel from each other, therefore, these regions do not have any effect on the other one [18].

There are many structures, which used both strained silicon and SOI techniques together. Most of the structures are based on the epitaxial growth of SiGe followed by another layer to generate SiGe-on insulator structure. Then strained silicon is grown on the surface to make the finale structure [19, 20]. Fig.4 shows the structure of the strained silicon on SiGe insulator.

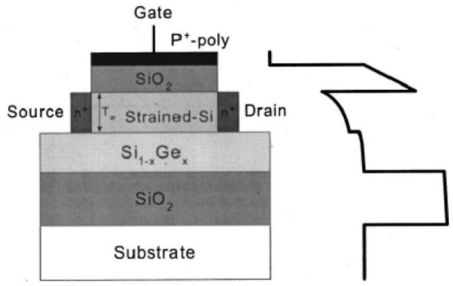

Fig. 4. Si/SiGe on insulator layer [21]

2.3. D) Multi-gate CMOS Transistor

The popular technique that influences the performance scaling, and speed of the CMOS based RF modules is a multi-gate transistor. Fig.5 shows the double gate (DG) metal–oxide–semiconductor field-effect transistor (MOSFET). Clearly, the structure has two gates, one at the bottom and another one at top. By acting field at both sides, controlling the transistor has been taking place efficiently. In addition, it is possible for more scaling the transistor, when two channels are interfaced in parallel and more current can be flown through the channel at given gate-source voltage.

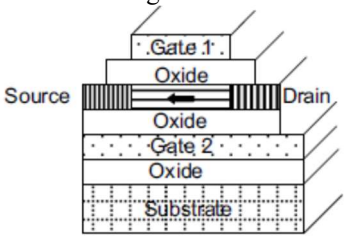

Fig. 5. Double Gate MOSFET [4]

In double-gate transistors, delay of both gates must be perfectly the same to modulate the channel in phase. It is difficult to fabricate these transistors horizontally. This issue can be addressed by applying laterally aligned gates. An upright illustration of this issue is DG-Fin-FETs and vertical double gates [22] which can be seen in Fig. 5a and 5b. By full depletion of Fins, more g_m/g_{ds} is achievable.

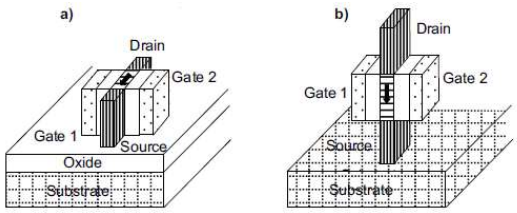

Fig. 6. a) double gates Fin b) vertical double gates FET [22]

More enhancements are reachable by using tri-state or ring gate structures, which is presented in Fig.6a and 6b. These processes are costly instead.

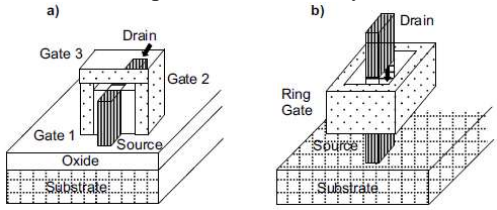

Fig. 7. a) Tri-gate Fin FET b) Ring gate FET [22]

To conclude, Table1.Shows comparison between Strained Silicon, SOI, and strained silicon-OI. As shown in table 1, strain silicon on insulator has benefits of both strain silicon and SOI together. Hence, this technique can be a practical method to make an efficent RF module. Beyond that perfomance of all these techniques are improved by multi-gate method.

3. Conclusion

The literature study has been conducted in CMOS scaling in recent years (2000-2013). The research paper reviewed the investigation about the scaling challenges faced with CMOS transistor fabrication and how to overcome the challenges. The arise issues are current leakage, low drain source small-signal output, and low voltage swing. It has been discussed about the complex troubles for scaling below 10*nm* and ways to delay stop scaling below 10*nm* such as SOI, strained silicon, high-k, and multi-gate transistors. The table of comparison among Strained Silicon, SOI and strained silicon-OI was provided. The table shows that the transistor performance can be improved by multi-gate technique.

Table 1: Comparsion Among Strained Silicon, SOI and strained silicon-OI

properties	**SOI**	**Strain silicon**	**Strain silicon SOI**
Circuit speed	fast	Very fast	Very fast
Power consumption	very low	low	Very low
Capacitance parasitic	low	high	low
Current leakage	low	high	low
Channel length scaling	good	good	good
Innovation	Structure innovation	Material innovation	Both material and structure innovation

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